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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
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ART UNIT	PAPER NUMBER
2117	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/803,792	NAM-JUNG HER	
	Examiner	Art Unit	
	Steven D. Radosevich	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *5,6 and 12-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-11 and 16-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-21 are present for examination. Acknowledgment is made that claims 5-6 and 12-15 have been canceled and that new claims 18-21 have been added. Claims 5-6 and 12-15 will not be given further consideration within the examination of claims 1-4, 7-11, and 18-21.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the not providing to a second group of data output pins the first and the second group of output signals during the first and the second test cycles must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. Examiner notes these features are claimed within the new claims 18 and 20 and support for these features is not found within the specification, indicating this is new matter.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering

of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 18-21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The claimed not providing to a second group of data output pins the first and second group of output signals during the first and second test cycles is not supported within the specification, and is thus viewed as new subject matter which is not described or disclosed within the specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-4, 7-11, and 18-21 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Godiwala et al (U.S. Patent 5712858).

1. As per claims 1, 7, and 16, Godiwala substantially teaches a semiconductor integrated circuit comprising:

A plurality of data output pins (C1 – C8 in figures 1-3;column 5 lines 40-45, and column 3 lines 1-5);

A data processing circuit to generate output signals responsive to in input signal (10 or Device Under Test in figures 1-3); and

An output selection circuit with at least a normal mode and a test made (16 in figures 1-3 and column 5 lines 40-45);

Where a first group of output signal are provided to a first group of data output pins in a first test cycle of the test mode (column 5 lines 40-55 and figures 1-3); and

Where a second group of output signals are provided to the first group of data output pins during a second test cycle of the test mode (column 5 lines 40-55 and figures 1-3).

Godiwala does not specifically teach an output selection circuit with at least a normal mode and a test made; where a first group of output signal are provided to a first group of data output pins in a first test cycle of the test mode; and where a second group of output signals are provided to the first group of data output pins during a second test cycle of the test mode.

However Godiwala discloses the claimed invention except for the output selection circuit being located within the semiconductor integrated circuit itself. It would have been obvious to one having ordinary skill within the art at the time the invention was made to have relocated the output selection circuit to within the semiconductor integrated circuit, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse,* 86 USPQ 70. Furthermore, those of ordinary skill within the art at the time the invention was made would recognize that by placing the output selection circuit within the semiconductor integrated circuit itself would require both a normal mode and test mode for the output selection circuit so that the semiconductor integrated circuit could operate appropriately within operating environment(s). Examiner notes that the output selection circuit reduces the pins/pads/connections required to test the semiconductor integrated circuit which would disable the semiconductor integrated circuit from operating appropriately within a system or device it is designed to operate in if placed within the semiconductor

integrated circuit itself as those of ordinary skill in the art at the time the invention was made would recognize, thus requiring the output selection circuit disabled, bypassed, or placed in operational (normal) mode when in non-test mode.

Therefore it would have been obvious to one or ordinary skill within the art at the time the invention was made to have been motivated to relocate the output selection circuit within Godiwala to within the semiconductor integrated circuit itself to allow a tester or test system that does not have an output selection circuit to test the semiconductor integrated circuit having more pins, thus avoiding the high cost of high pin count tester as indicated within Godiwala (column 2 lines 17-29 and column 2 line 51 – column 3 line 42).

2. As per claims 2 and 8, Godiwala teaches the semiconductor integrated circuit wherein the output selection circuit repeats the first and second test cycles during testing (column 5 lines 40-55 and figures 1-3).

3. As per claims 3, 4, 9, 10, 11, 17, and 18-20, Godiwala teaches the semiconductor integrated circuit wherein the output selection circuit sends odd output signals to odd/even data output pins during the first cycle of the test mode; and wherein the output selection circuit sends even output signals to odd/even data output pins during the second test cycle of the test mode (column 5 lines 40-55 and figures 1-3).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

i. Ozawa (U.S. Publication 20050166113 A1) discloses multiple outputs, each being selected at different test cycles for inclusion within a single signal during a single test period. See specifically figure 2 with respect to figure 1.

ii. Deb (U.S. Patent 6971045) discloses switch matrix used to reduce pins required by a tester to test a DUT along with the switch matrix being within the semiconductor integrated circuit, thus disclosing the switch matrix that operates as the output selection circuit requiring an operational mode and test mode so as not to disable the semiconductor to operate appropriately within a system or device it is designed to operate in.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven D. Radosevich whose telephone number is 571-272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Cynthia H. Britt can be reached on 571-2723815. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven D. Radosevich
Examiner
Art Unit 2117

CYNTHIA BRITT
PRIMARY EXAMINER